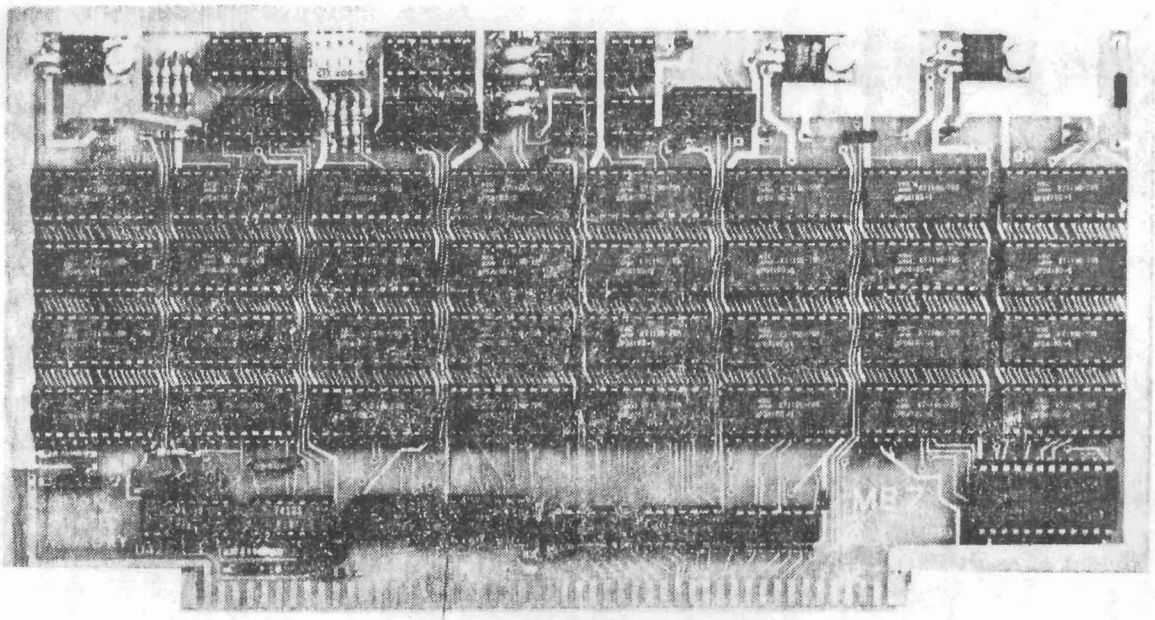
Solid State Music

S# 206 Purchased 8/6/78 MB7 S-100

16K STATIC RAM BOARD



FEATURES

S-100 bus compatible.

Fully buffered address & data lines.

Extra lo-power, 200nsec 4K x 1-bit static RAMs allow operation over 2MHZ.

Board inhibit line allows hardware jumps on reset or power-up and/or memory expansion beyond 64K.

Address selection at any 4K boundry with DIP switch at top of board.

Memory protect in 4K blocks with automatic unprotect on power-up.

T.I. lo-profile sockets for all ICs.

Hi-grade glass-epoxy board with gold contacts.

PARTS

1- 74L00
4- 74L04
1- 7483
1- 74LS32
1- 74(LS)47
1- 7442
1- 7481A
1- 74121
1- DM8098 or 74368
1- 8212
32- uPD410
4- MM0026
1- 7812 or 340T-12 12V regulator
2- 7805 or 340T-5 5V regulators
1- 1N751 or 1N5231 5V zener
1- 560 ohm ½ watt resistor
1- 68 ohm ¼w 5%
1- 100 ohm ¼w
6- 1.0K ¼w
10- 4.7K ¼w 5%
1- 3.92K 1% RN55-type

4- 100pF disc capacitors
1- .001uF ceramic disc
18-.1uF ceramic

1- 100pf 5%
1- .0033uF 5%
2- 2.7uf @ 20V tantalum
1- 4 position DIP switch
1- heat sink
3- sets #6 hardware
1- PC Board
4- 8 pin sockets
1- 24 pin socket
4- 16 pin sockets
8- 14 pin sockets
32- 22 pin sockets

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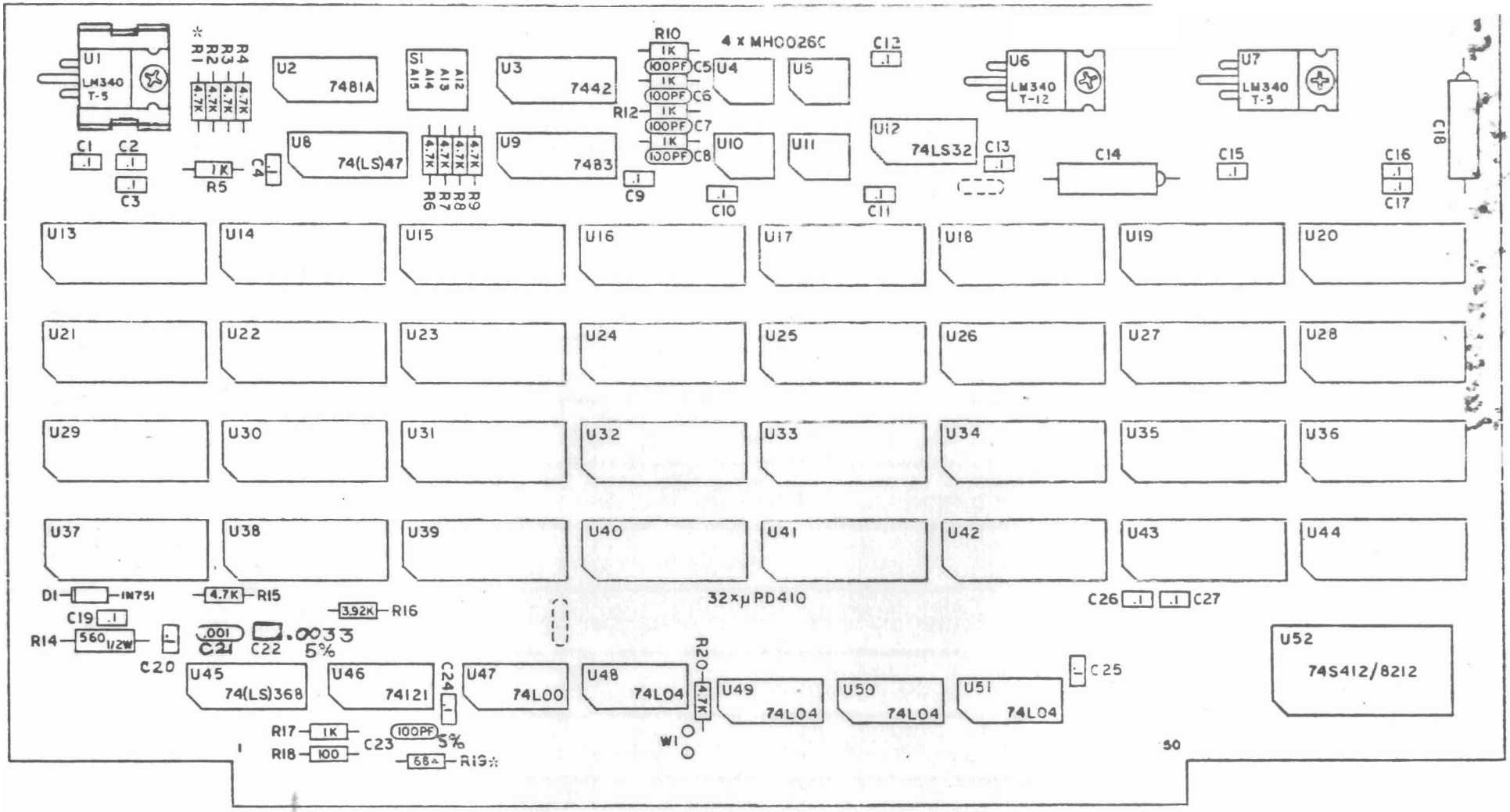
MB7 - 16K STATIC MEMORY BOARD

1.0 ASSEMBLY INSTRUCTIONS (refer to Figure 1)

- ☐ Check kit contents against parts list.
- ☐ Check PC board for possible warpage and straighten if required.
- ☐ Insert 32 22-pin sockets into the component side of the board with the "pin 1" index toward the left of the board. (The component side is the side on which "Solid State Music" is printed.)
- ☐ Insert 1 24-pin, 4 16-pin, 8 14-pin, and 4 8-pin sockets. DON'T SOLDER!
- ☐ Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.
- ☐ Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all of the sockets pins are through the holes.)

  Note: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or sponge.
- ☐ On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.
- ☐ Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on top while reheating each soldered pin.
- ☐ Complete soldering the remaining pins of each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip against the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron tip is recommended.
- ☐ Insert and solder 1 ½w and 19 ¼w resistors in their respective locations.
- ☐ Observing polarity, insert and solder zener diode.
- ☐ Insert and solder 18 .1uF ceramic capacitors.
- ☐ Insert and solder 2 5% timing capacitors.
- ☐ Insert and solder 5 ceramic disc capacitors in their respective locations.



*NOTES: 1) Allow clearance for heatsink when installing R1.

2) Allow clearance for edge connector when installing R19.

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16K STATIC RAM

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1.0 ASSEMBLY INSTRUCTIONS (continued)

☐ Observing polarity, insert and solder 2 tantalum capacitors.

☐ Insert DIP switch with the ON position toward the top of the board. Solder. (OPEN position towards the bottom.)

☐ Place regulators on the board so the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending position to match the board holes--allow for a bend radius.

☐ Bend regulator leads to match holes in board.

☐ If available, apply thermal compound to the back side of each regulator case (the part that lies flat against the board).

☐ Drop regulators in place on front of board, insert #6 screws from front, and secure firmly with lock washer and nut. Note: heat sink goes under U1.

☐ Solder regulator leads to pads on back of board. Do not use excessive heat.

2.0 FUNCTIONAL CHECK

WARNING! DO NOT INSTALL OR REMOVE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD OCCUR.

☐ Apply power (+8 volts approx.) to board by plugging into computer or by connection to a suitable power supply. Measure the outputs of the +5V regulators. If less than 4.8 volts is measured (allowing for meter accuracy) check for shorts or wiring errors. CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY-KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS AND SUBSEQUENT TESTS!

☐ Apply power (+16 volts) to the board by plugging into computer or by connection to a suitable power supply. Verify that the output of the +12V regulator is between +11.5 & 12.5 Vdc.

☐ Apply power (-16 volts) to the board by plugging into computer or by connection to a suitable power supply. Verify that the voltage across D1 is between -4.5 & 5.7 Vdc.

☐ Now look the board over carefully. Check for poor solder joints or bridges. Using the component layout drawing, look for improper part locations or polarity. A few minutes of careful inspection may save a few hours of troubleshooting.

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2.0 FUNCTIONAL CHECK (continued)

☐ Observing polarity, insert all support chips into their sockets along with the first row (4K) of RAMs. (Top row.)

☐ Set A15 thru A12 to "OFF" (this addresses the board to ØØ hex.)

☐ Install board. Remember, this board, addressed per above setting, must have the first 16K uncontested. Any boards addressed for the first 16K positions must be readdressed or removed.

☐ "Examine" ØØ hex and verify that the memory is not protected.

☐ Manually program with the front panel to verify that data can be stored.

☐ Power-down computer and install last 3 rows of RAMs.

☐ "Examine" 00,10,20, & 30 hex and verify that the memory is not protected.

☐ Program a few locations in each 4K block from the front panel to verify memory operation.

3.0 SET-UP

3.1 Address Selection (S1)

The board is designed to be 16K contiguous bytes of memory starting at any 4K boundary. Starting address is easily selected using the four position DIP switch at the top of the board.

Switches should be set to represent the four high order bits of the starting address, with OFF representing a zero and ON representing a one.

Starting Address (HEX)	DIP Switch Settings A15	A14	A13	A12	Memory Range (Approx. decimal)
0000	OFF	OFF	OFF	OFF	0 - 16K
1000	OFF	OFF	OFF	ON	4 - 20K
2000	OFF	OFF	ON	OFF	8 - 24K
3000	OFF	OFF	ON	ON	12 - 28K
4000	OFF	ON	OFF	OFF	16 - 32K
C000	ON	ON	OFF	OFF	48 - 64K
D000	ON	ON	OFF	ON	52 - 64K & 0 - 4K
E000	ON	ON	ON	OFF	56 - 64K & 0 - 8K
F000	ON	ON	ON	ON	60 - 64K & 0 - 12K

4 = 0100
8 = 1000

Note that card addressing is cyclical, i.e. address 0000 follows FFFF when starting address is above D000 (hex).

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4.0 APPLICATIONS

4.1 Board Select Feature

4.1.1 General

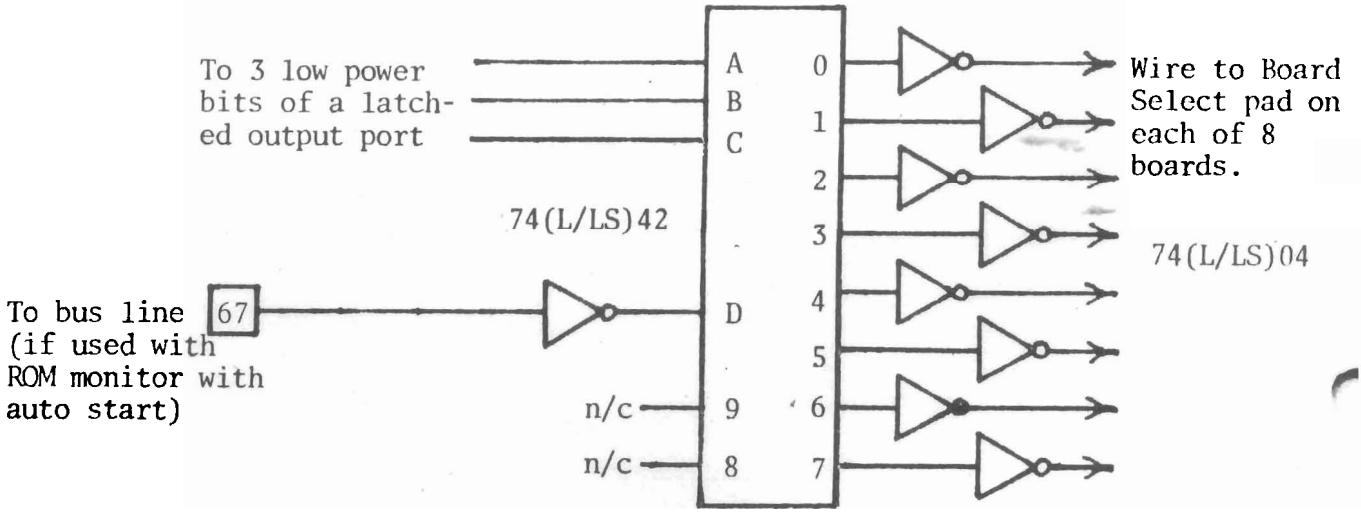
A board select, or "phantom" line is provided on the MB7 which adds considerably to its versatility. This line comes out on a pad at the bottom of the board below and between U48 & U49. Directly below is another pad connected to pin 67 of the bus. A short jumper is all that is required to connect the board select line to pin 67 of the bus; or, this line may easily be connected to any other unused bus pin. Pulling the board select line low disables the MB7.

4.1.2 Hardware Jumps

The board select line may be used in conjunction with jump-on-reset and/or jump-on-power-up circuitry (which is available on certain ROM & ROM/RAM boards such as SSM's MB9). This circuitry disables the computer's memory while it jams a jump instruction onto the bus. The end result is a computer whose monitor program (or other software) comes on-line when it is reset and/or powered-up.

4.1.3 Memory Expansion

The suggested circuit below, when connected to any latched output port (and is easily added to any Solid State Music IO-2 board) will allow up to eight 16K boards to share the same address. Up to 128K of memory can actually share the same address using this circuit. Each time a different three bit combination is sent to the three low order bits of the output port, a different 16K board will be selected, resulting in "bank switching."



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5.0 TROUBLE SHOOTING HINTS

5.1 General

a. Check for proper settings of DIP switches.

b. Verify that all ICs are in the correct sockets.

c. Visually inspect all ICs to be sure that leads are in the socket and not bent under.

d. Verify that the output voltage of each regulator is correct.

e. Inspect back side of board for solder bridges, running a small sharp knife blade between traces that appear suspicious. A magnifying glass is a must for this.

f. If you have an addressing problem:

1) Check U9 (7483) for addresses A12 thru A15 as well as proper outputs.

2) Check inputs & outputs of buffers U48 thru U50 (74L04) for addresses A0 thru A11.

g. If you have a problem with data output (consistent missing bits):

1) Check inputs & outputs of buffers U50 & U51 (74L04) for shorts as well as proper operation.

2) Check signals on U52 (8212)

h. If memory does not protect/unprotect properly:

1) Check addressing per f.1.

2) Check inputs and outputs of U8 (7447) and U2 (7481).

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5.0 TROUBLE SHOOTING HINTS (continued)

5.2 Timing

Note: An oscilloscope with at least 20MHZ bandwidth should be used for all timing measurements.

a. MWRITE delay

In order to achieve reliable front panel operations in certain mainframes (primarily IMSAI), it was necessary to delay MWRITE. This delay, as measured from pin 6 to 5 of U45 on the leading (negative) edge at a 2V level, should be 175 +25 nsec. This delay may be adjusted by changing the value of R19.

b. Chip Enable duration

The pulse duration at the output (pin 6) of the 1-shot (U46) should be 275 + 25 nsec (measured at a 2V level). If the Chip Enable pulse is too short, unreliable operation may result.

6.0 THEORY OF OPERATION

6.1 General

The MB7 was designed using the NEC uPD410 4K x 1 bit static MOS random access memory. Four rows of 8 ICs form a 16K byte memory.

6.2 Addressing

The 12 least significant address bits are buffered and directly drive 12 address pins on the memory IC's. The starting address as selected by the four position DIP switch is effectively subtracted from the four high order address bits to provide a "board selected" output (at pin 8 of the OR gate) and two signals which drive a 7442 used as a 1 of 4 decoder. The 7442 determines which one of the four rows of memory IC's (if any) will be selected by driving one of four 12 volt Chip Enable drivers.

6.3 Chip Enable

Each Memory IC has an enable line which must be brought to a logic one state to start each memory cycle. A one-shot monostable generates a 275 nanosecound pulse for this purpose. Since the memory IC's data is valid only when the Chip Enable signal is high, the output data is latched into an 8212. The memory IC's draw little power when not enabled, so by enabling only one of the four rows at a

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6.0 THEORY OF OPERATION (continued)

6.3 Chip Enable (continued)

time (and for only 275 ns), power drain is kept to a minimum: typically 550 ma from the 8 volt bus and 80 ma from the 16 volt bus.

6.4 Triggering

For memory read cycles the Chip Enable signal is triggered from PSYNC and $\emptyset 1$. For memory write cycles the triggering signal is MWRITE, which is delayed approximately 180 ns to insure proper operation when using the front panel deposit switch. Some of the timing relationships are shown on the following page.

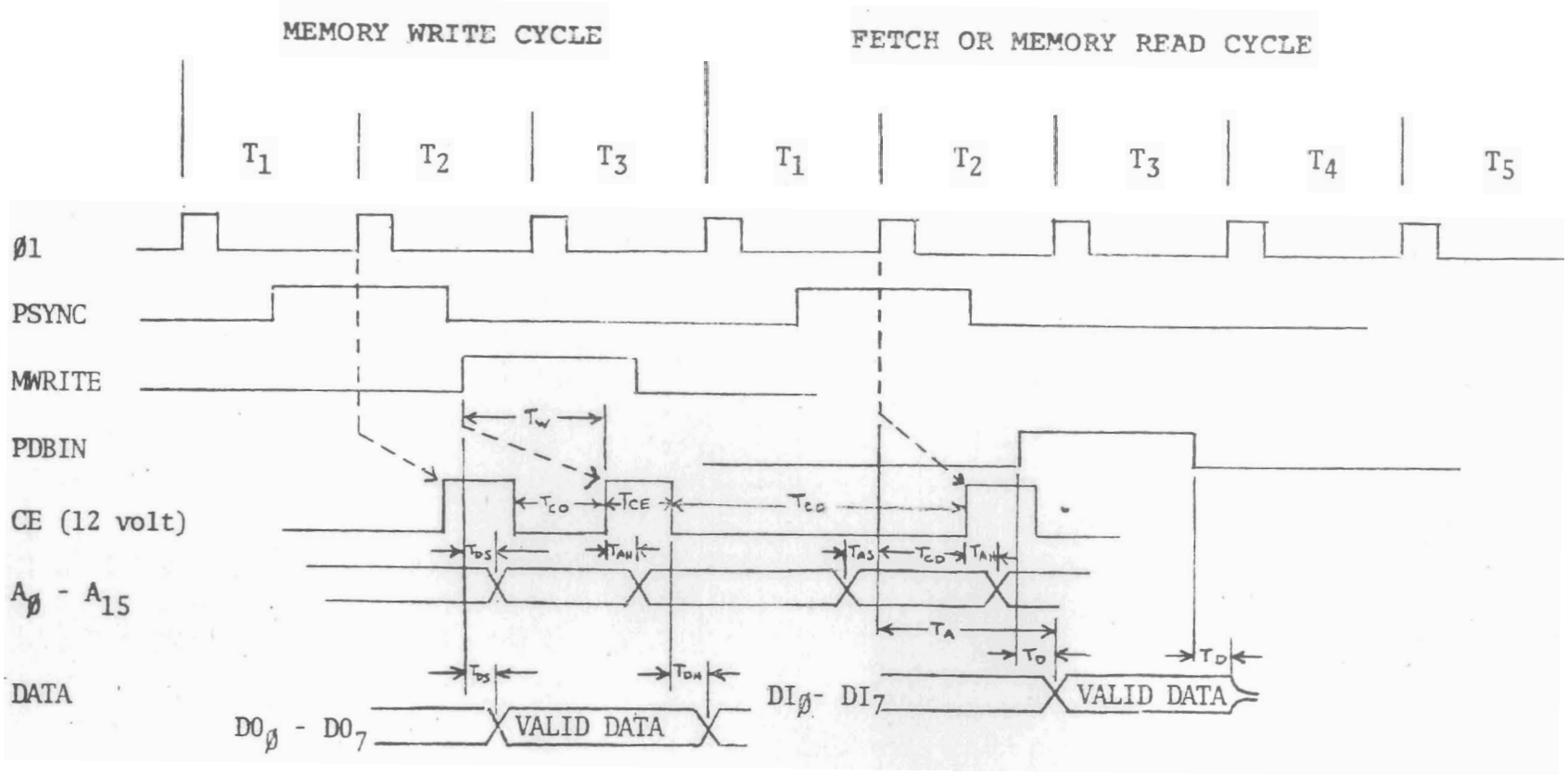
6.5 Memory Protect

A 16 bit memory IC (7481), of which only four bits are used, is the heart of the memory protect feature. Each bit controls a 4K block of memory on the card and can be set or reset from the front panel PROTECT/UNPROTECT switch. All bits are initially set to the unprotect state by the $\overline{\text{POC}}$ signal when power is first applied to the computer. The 74LS47 acts as an address decoder for the matrixed address lines of the 7481.

7.0 WARRANTY

Parts guaranteed to original purchaser for 90 days, unless failure is due to misuse or failure of purchaser to exercise caution in assembly and operation. Registration card must by returned at time of purchase to validate warranty.

Assembled boards may be returned for service. A service charge will be be made unless, in our judgement, the problem is due to a defective board or parts.


MEMORY WRITE CYCLE
FETCH OR MEMORY READ CYCLE
T1
T2
T3
T1
T2
T3
T4
T5
ø1
PSYNC
MWRITE
PDBIN
CE (12 volt)
Aø - A15
DATA
DOø - DO7
VALID DATA
DIø - DI7
VALID DATA
TW
TCO
TCE
TCO
TDS
TAH
TAS
TCD
TAH
TA
TO
TD
TDS
TDH

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		minimum	typical	maximum
MEMORY WRITE CYCLE TIMING				
t_{DS}	data set-up delay from MWRITE			100ns
t_W	CE delay from MWRITE		270ns	320ns
t_{DH}	data hold time	50ns		
t_{AH}	address hold time	80ns		
MEMORY READ CYCLE TIMING				
t_{AS}	required address set-up prior to ϕ_1	50ns		
t_{CD}	CE delay from ϕ_1		90ns	120ns
t_A	data access time from ϕ_1		240ns	320ns
t_D	delay to valid data on bus			60ns
t_{AH}	address hold time	80ns		
	CE duration	250ns	275ns	300ns
t_{CO}	timing between CE pulses	190ns		

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MB-7 M.T.W. 11-2-77

ERRANTA SHEET

Do you have a MB-7 serial-B board?

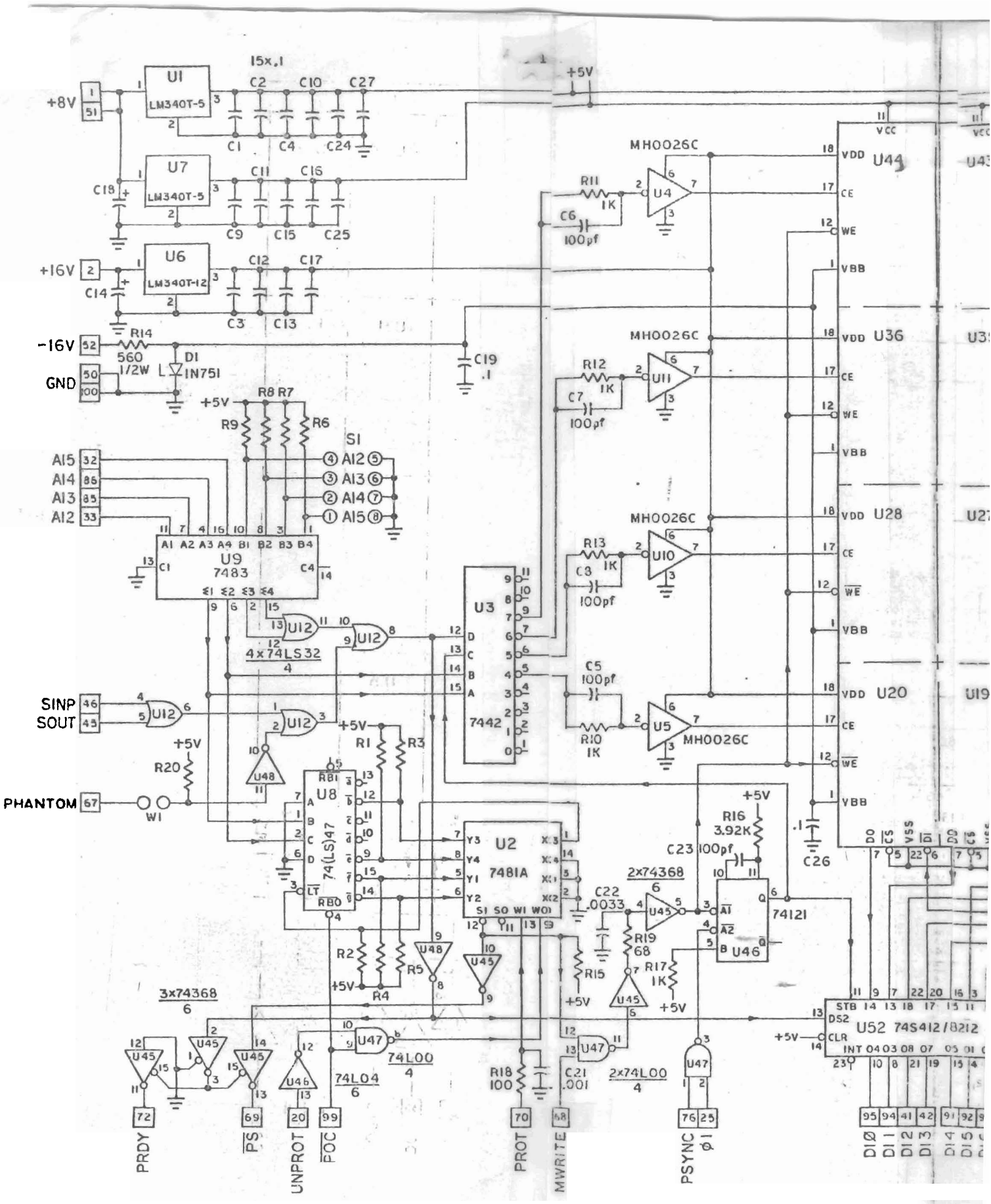
If you do, then there are two connections missing. Sorry.

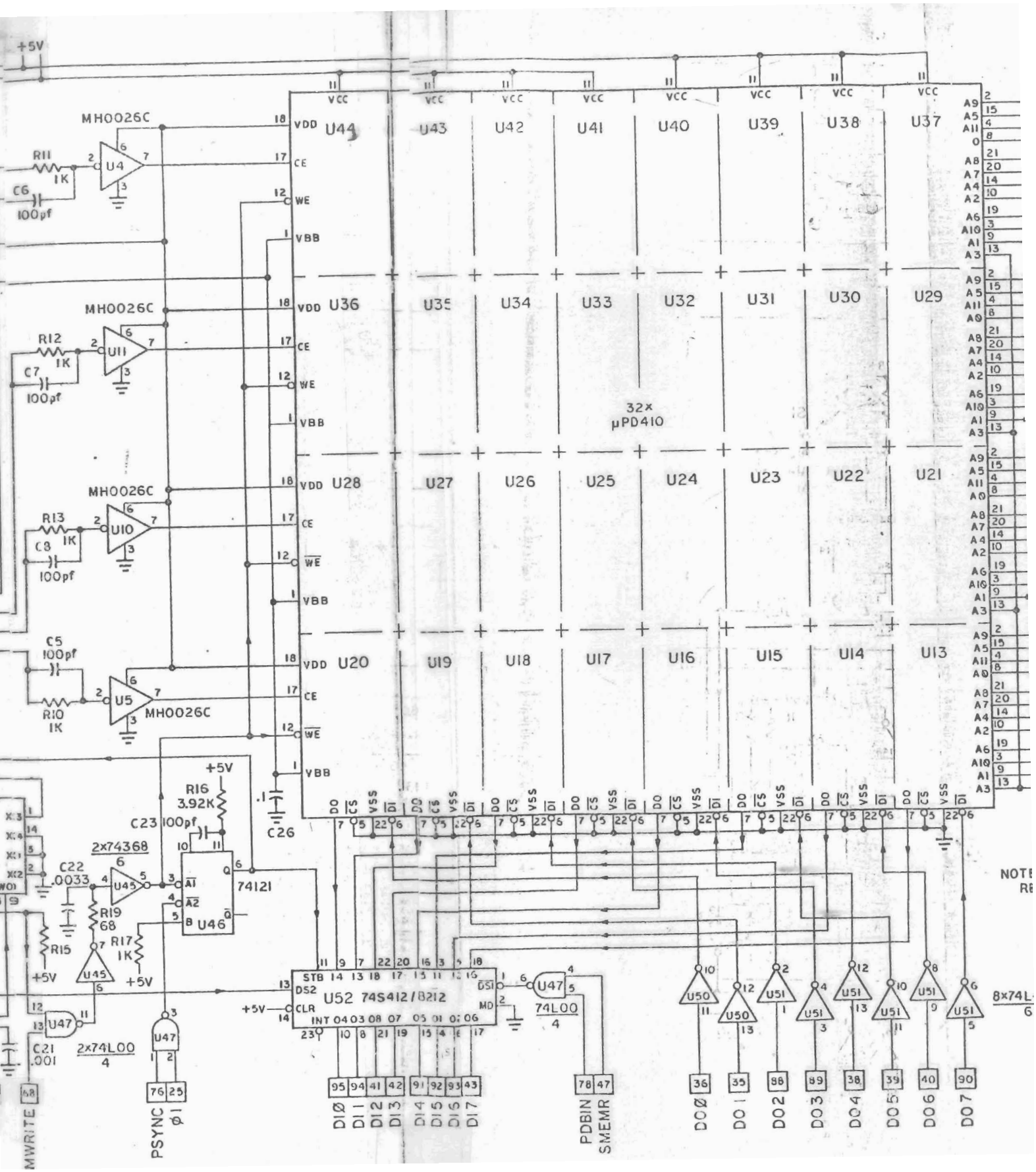
Please make the following connections with insulated jumper wires.

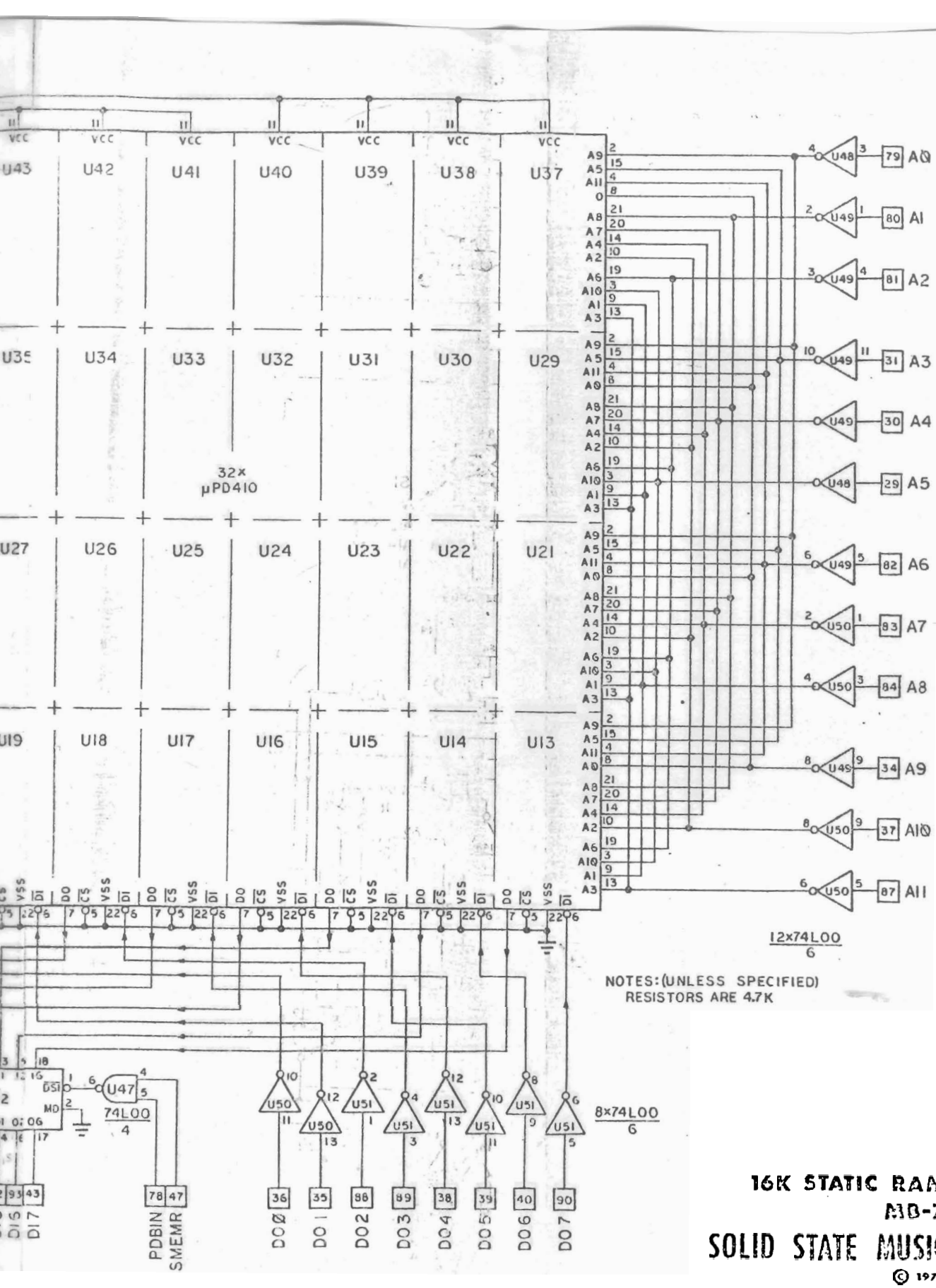
CONNECT:

U19, pin 3 to U20, pin 3.

U27, pin 8 to U28, pin 8.


+8V
+16V
-16V
GND
U1
LM340T-5
U7
LM340T-5
U6
LM340T-12
C1
C2
C3
C4
C9
C10
C11
C12
C13
C15
C16
C17
C18
C24
C25
C27
R14
560
1/2W
D1
IN751
C19
.1
+5V
MH0026C
U44
U36
U28
U20
R11
R12
R13
R10
1K
C6
C7
C8
C5
100pf
U4
U11
U10
U5
VDD
CE
WE
VBB
VCC
SINP
SOUT
PHANTOM
W1
R20
R1
R2
R3
R4
R5
R6
R7
R8
R9
S1
AI2
AI3
AI4
AI5
U9
7483
U3
7442
U12
4x74LS32
U48
U8
74(LS)47
U2
7481A
U45
U46
U47
2x74368
3x74368
74LS00
74L04
R16
3.92K
C23
C22
.0033
R19
68
R17
R15
R18
100
C21
.001
74121
U52 74S412/8212
STB
DS2
CLR
INT
PRDY
PS
UNPROT
POC
PROT
MWRITE
PSYNC
ø1
DI0
DI1
DI2
DI3
DI4
DI5


+5V
MH0026C
R11 1K
C6 100pf
U4
R12 1K
C7 100pf
U11
R13 1K
C8 100pf
U10
C5 100pf
R10 1K
U5
VDD
CE
WE
VBB
U44
U43
U42
U41
U40
U39
U38
U37
U36
U35
U34
U33
U32
U31
U30
U29
U28
U27
U26
U25
U24
U23
U22
U21
U20
U19
U18
U17
U16
U15
U14
U13
32x
μPD410
R16 3.92K
C23 100pf
C26 .1
2x74368
6
C22 .0033
R19 68
R15
R17 1K
U45
U46
74121
U52 74S412/8212
STB
DS2
CLR
INT
DS1
MD
U47
74L00
4
2x74L00
4
C21 .001
MWRITE
PSYNC
φ1
PDBIN
SMEMR
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
U50
U51
8x74L
NOTE
R



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